1. (original) A computer system, comprising:

a cache memory that reads and caches a group of lines with a single memory transaction; and

a system for maintaining identity of which device, if any, owns the group of lines, and which device, if any, owns each individual line within the group of lines.

2. (canceled)

3. (original) The computer system of claim 1, further comprising:

at least two lines in the group of lines having separate owners.

4. (original) A computer system, comprising:

a cache memory that reads a group of lines with a single memory transaction; and

the cache memory receiving fewer than all lines within the group of lines, when the group of lines is requested, and when the group of lines is partially owned by another cache memory.

5- 6 (canceled)

7. (original) A method of maintaining coherency for a computer system, comprising:

retrieving a group of lines in response to a request for a single line; and

maintaining ownership information for the group of lines and for each individual line within the group of lines.

8. (original) A method of transferring lines of memory in a computer system, comprising:

requesting, by a processor, a line of memory;

copying, from a shared memory, to a cache memory, the line of memory requested;

copying, from the shared memory to the cache memory, all additional unowned lines within a group of lines corresponding to the requested line, and not copying any owned lines, other than the requested line, within the group of lines.

9. (original) The method of claim 8, further comprising:

setting a coherency state, within the cache memory, of an entry location for a line in the group of lines that is not copied, to a state that indicates that the contents of the entry location are invalid.

10. (original) A method for maintaining coherency for a computer system, comprising:

(a) requesting, by a processor, a line of memory, the line of memory within a group of lines;

(b) detecting that all lines in the group of lines have been modified by one owner;

(c) copying, in response to the request of step (a), all the lines in the group of lines to a cache memory for the processor; and

(d) setting a coherency state, within the cache memory, of all lines in the group of lines, to a state that indicates that the lines are owned by the cache memory.